

Fig. 1a

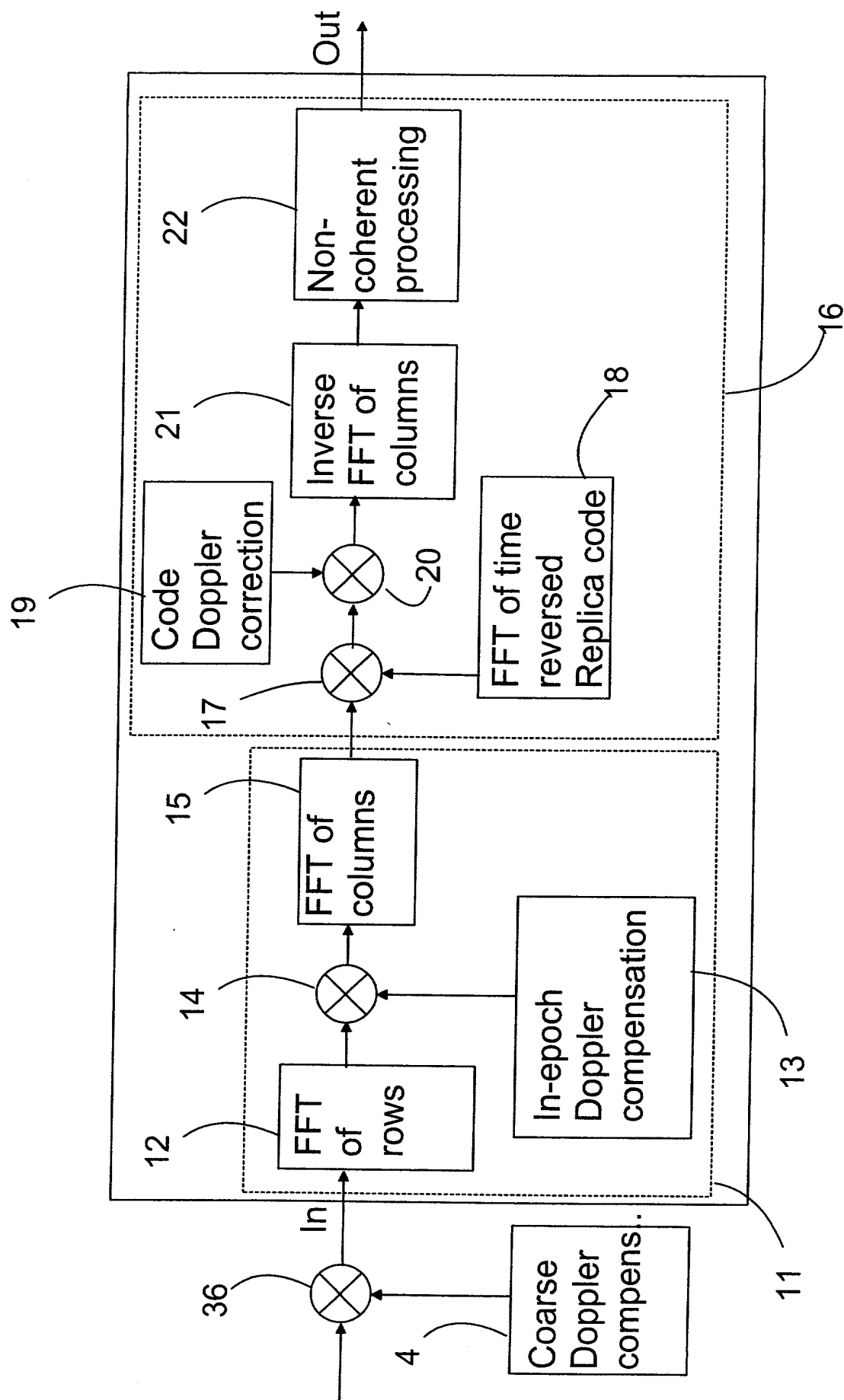


Fig. 1b

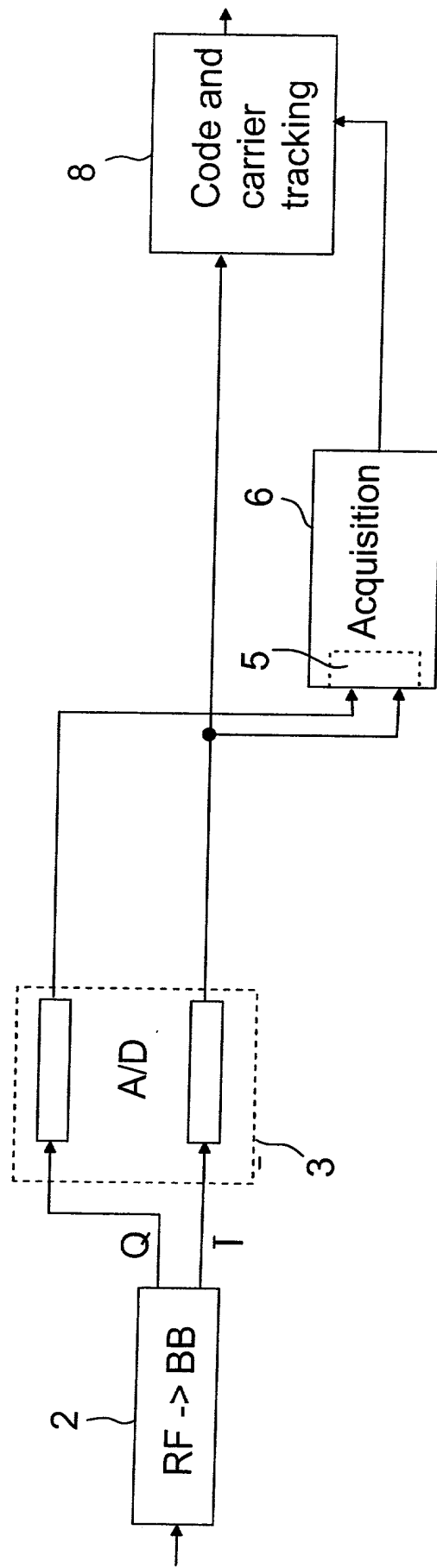


Fig. 1c

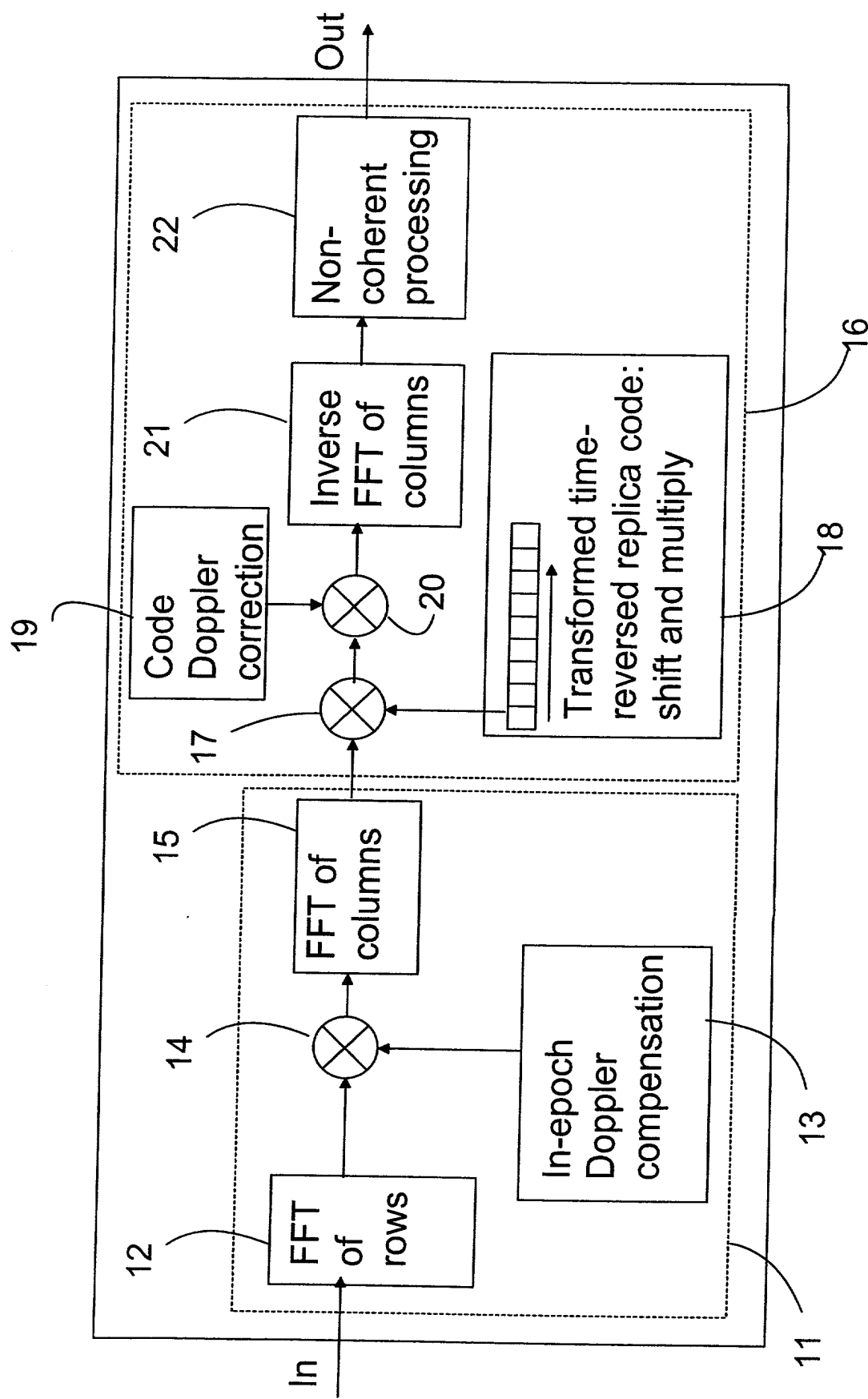


Fig. 1d

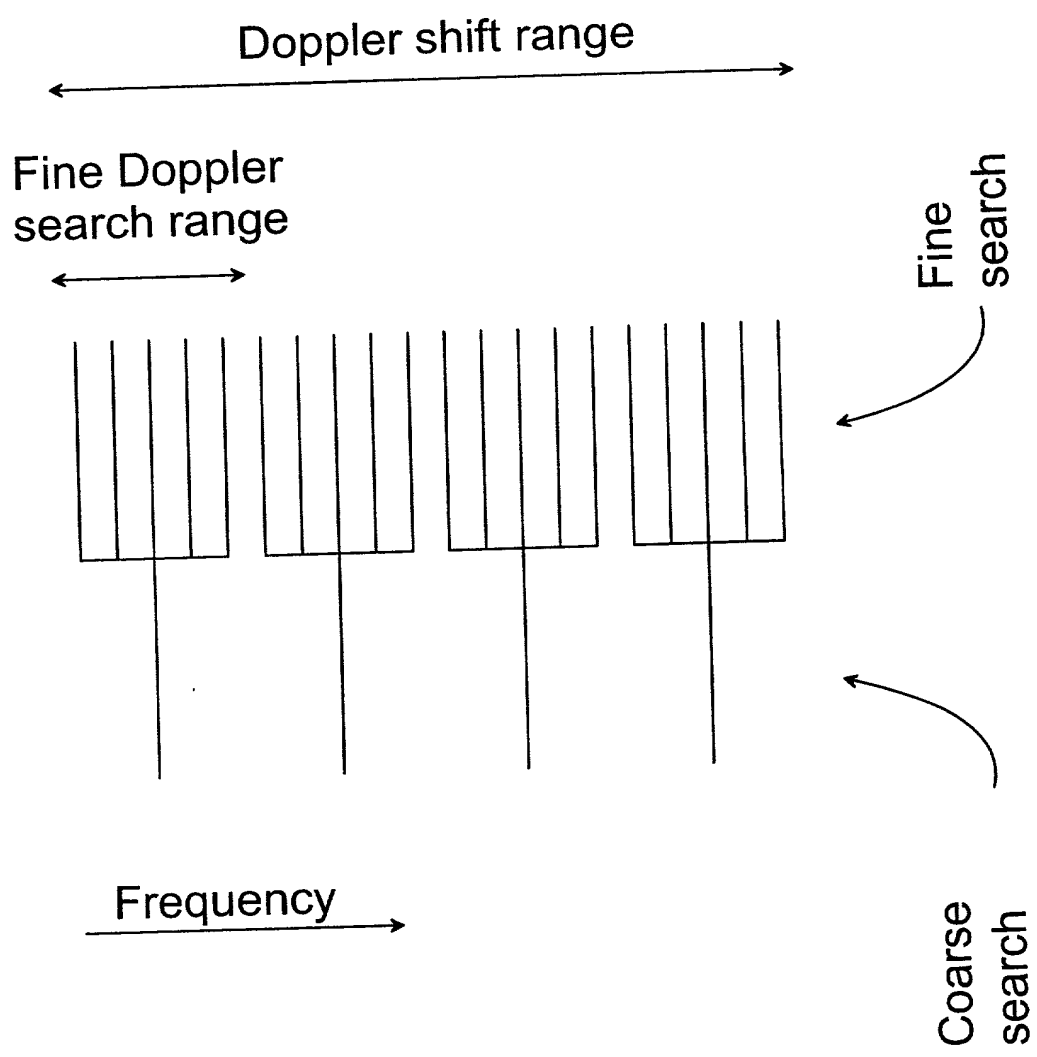


Fig. 2a

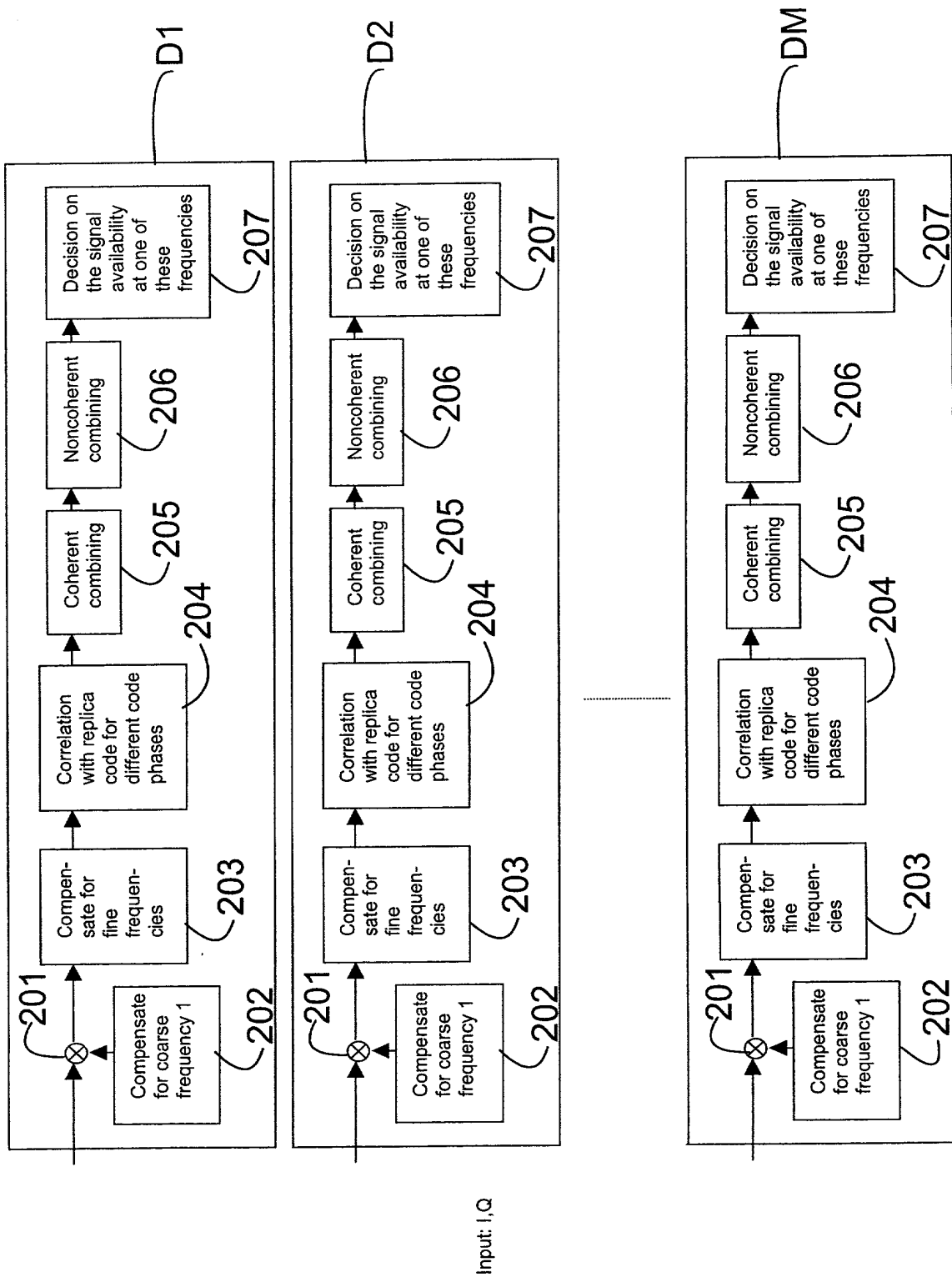


Fig. 2b

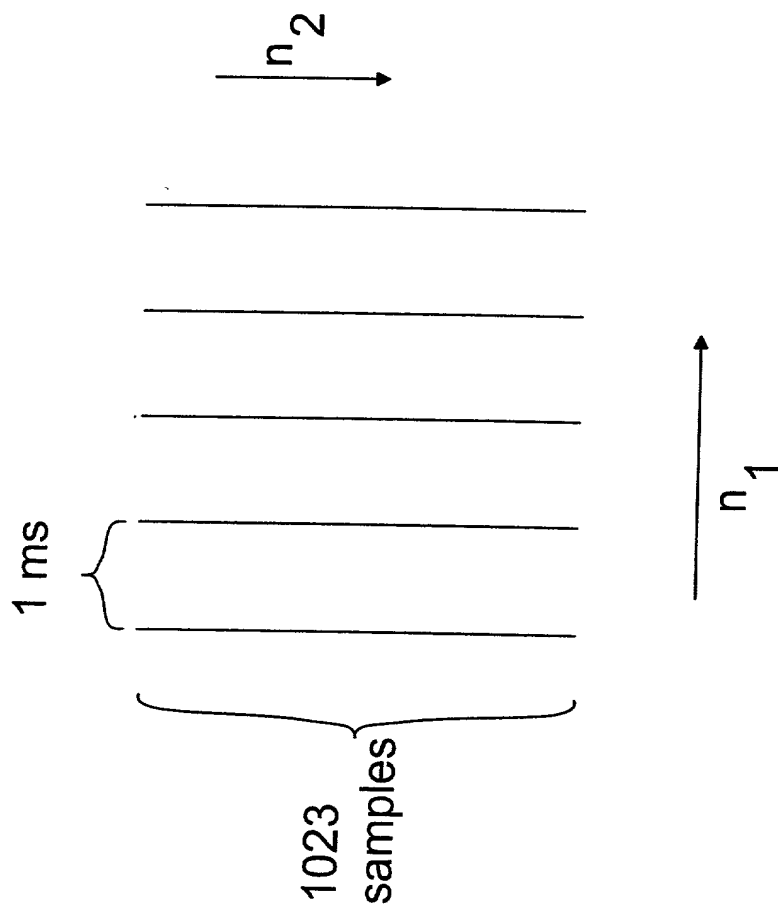


Fig. 3

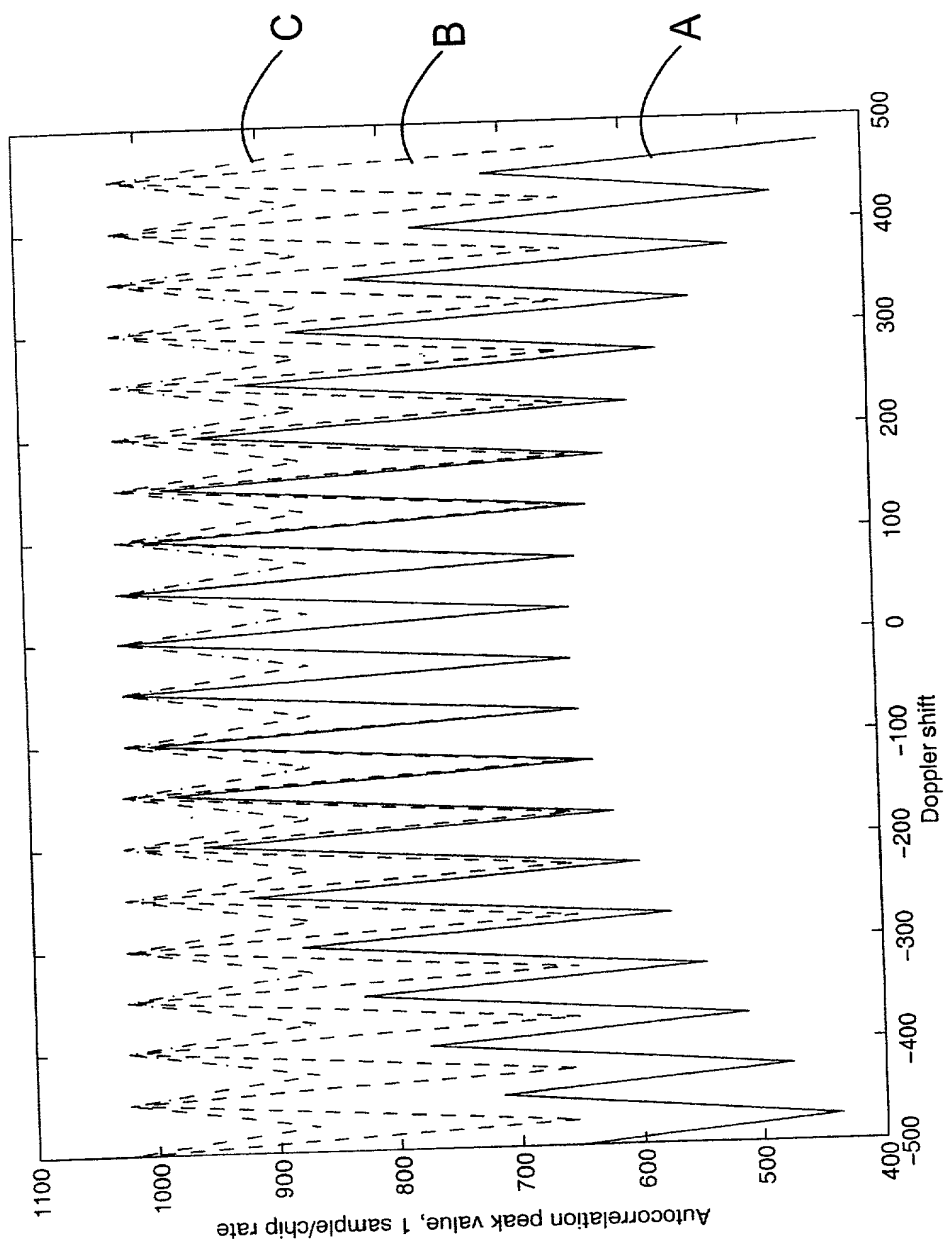


Fig. 4

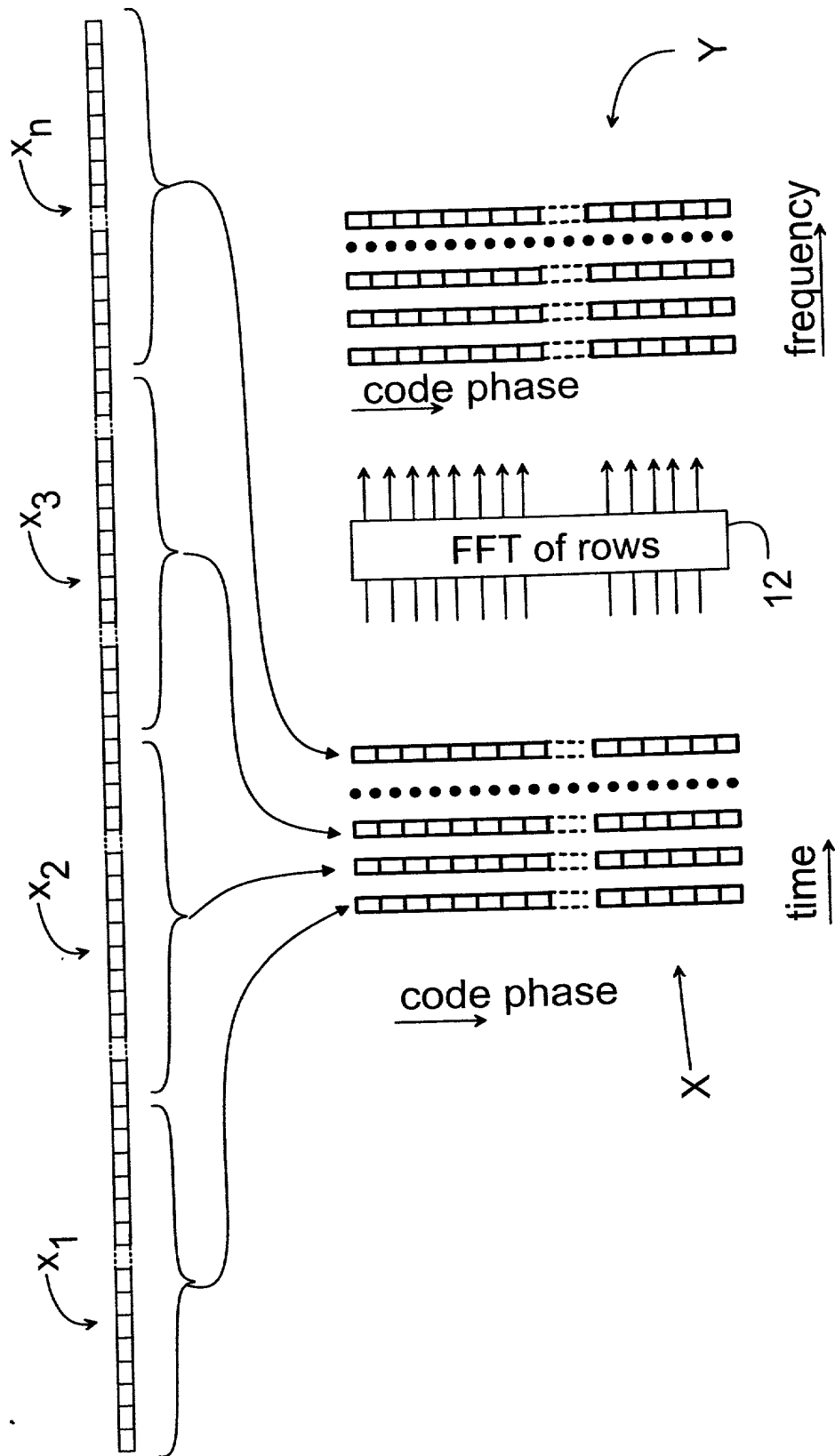


Fig. 6 is a block diagram of a code phase locked loop (CPLL) system. The system includes a code generator 10, a phase-locked loop (PLL) 12, a multiplier 14, and a code phase detector 16. The code generator 10 provides a code phase signal to the PLL 12. The PLL 12 provides a frequency signal to the multiplier 14. The multiplier 14 multiplies the code phase signal by the frequency signal to produce a code phase locked signal. The code phase detector 16 receives the code phase locked signal and provides a code phase error signal to the PLL 12.

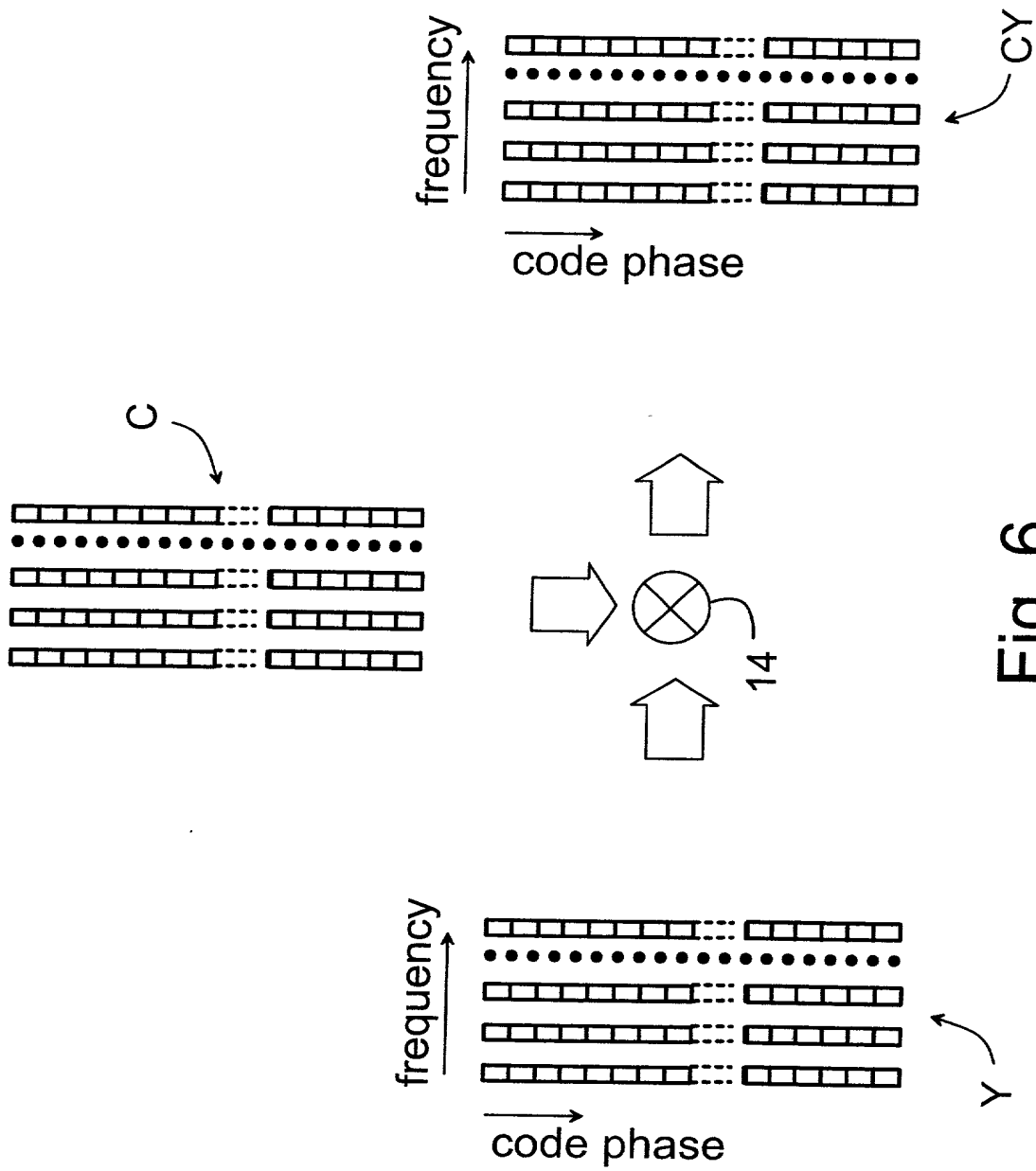


Fig. 6

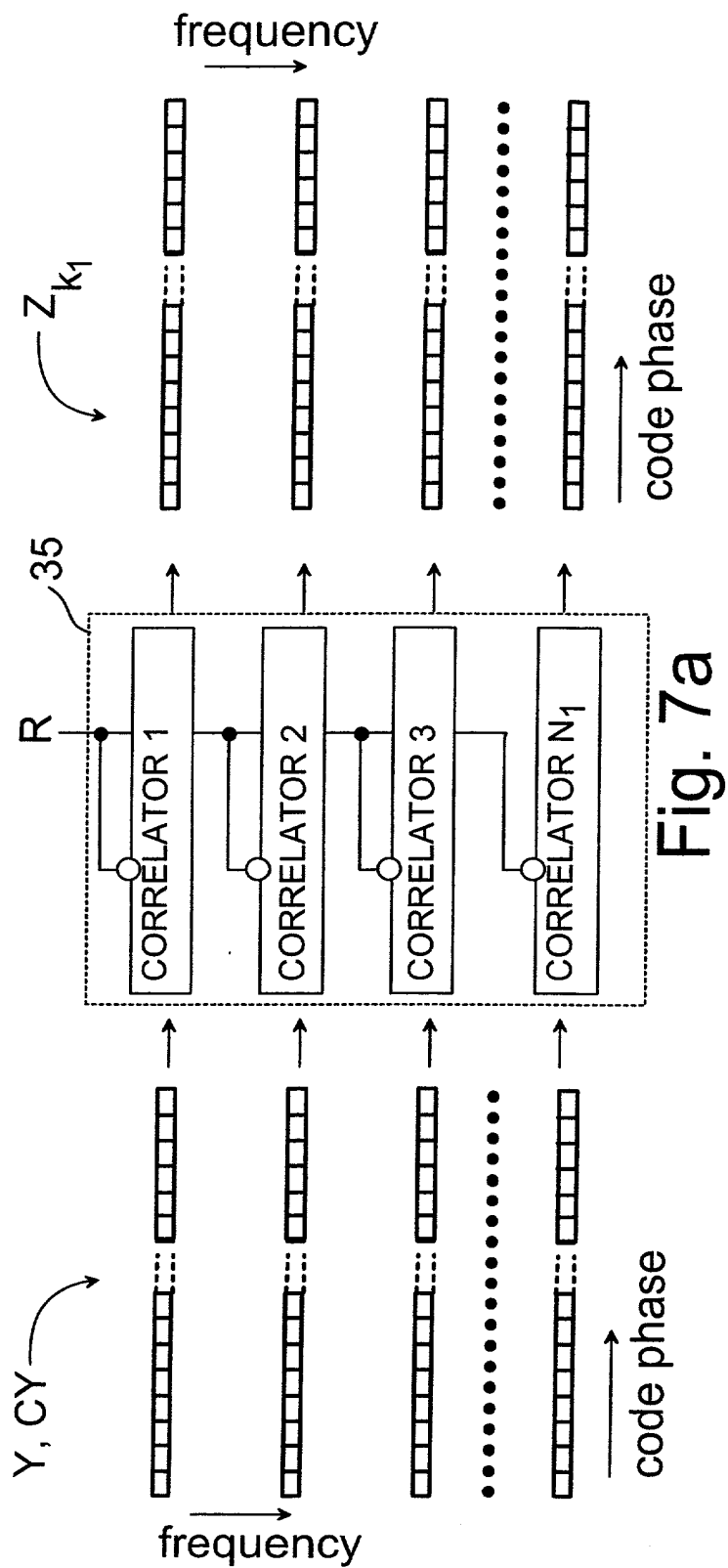


Fig. 7a

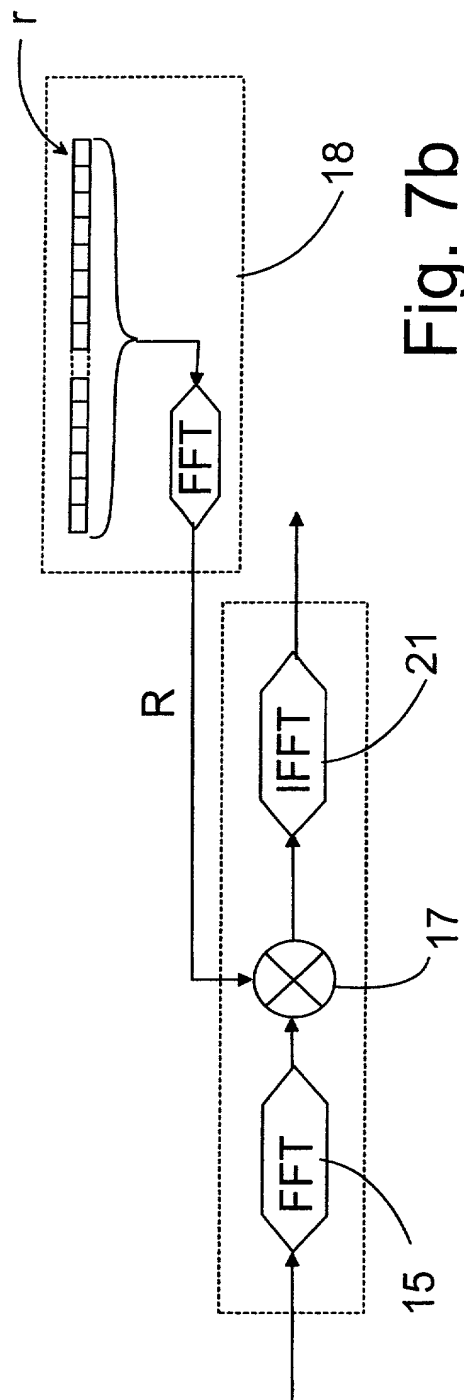


Fig. 7b

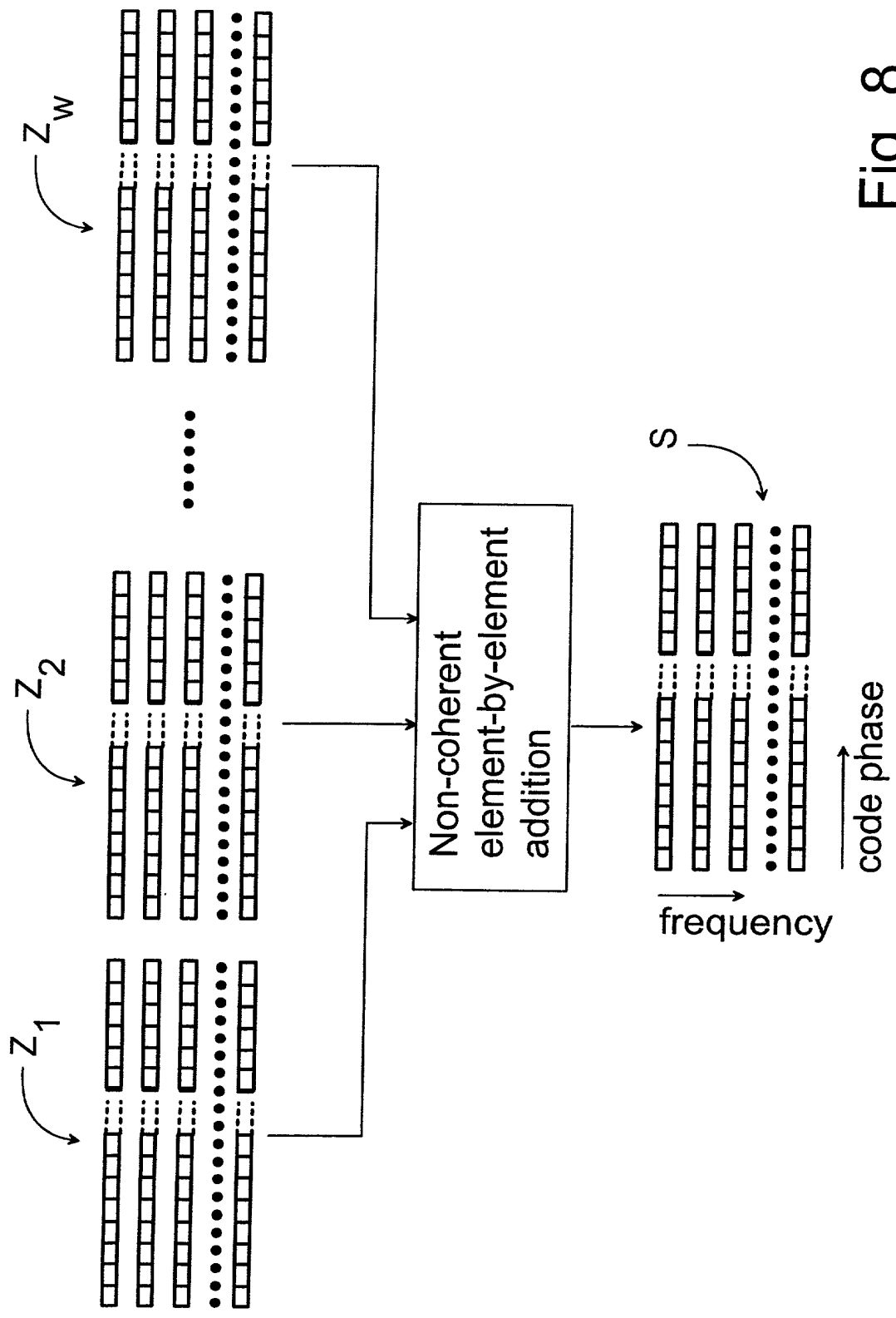


Fig. 8

Fig. 10 is a 3D plot showing the autocorrelation peak value as a function of code phase and Doppler frequency. The vertical axis represents the autocorrelation peak value, ranging from 0 to 1200. The horizontal axis represents the code phase in the range [0...1023], ranging from 0 to 1200. The depth axis represents the Doppler frequency in the range [-5...6] kHz, ranging from -6 to 6. The plot shows a dense, elongated surface of data points, indicating a strong correlation across the entire range of code phase and Doppler frequency.

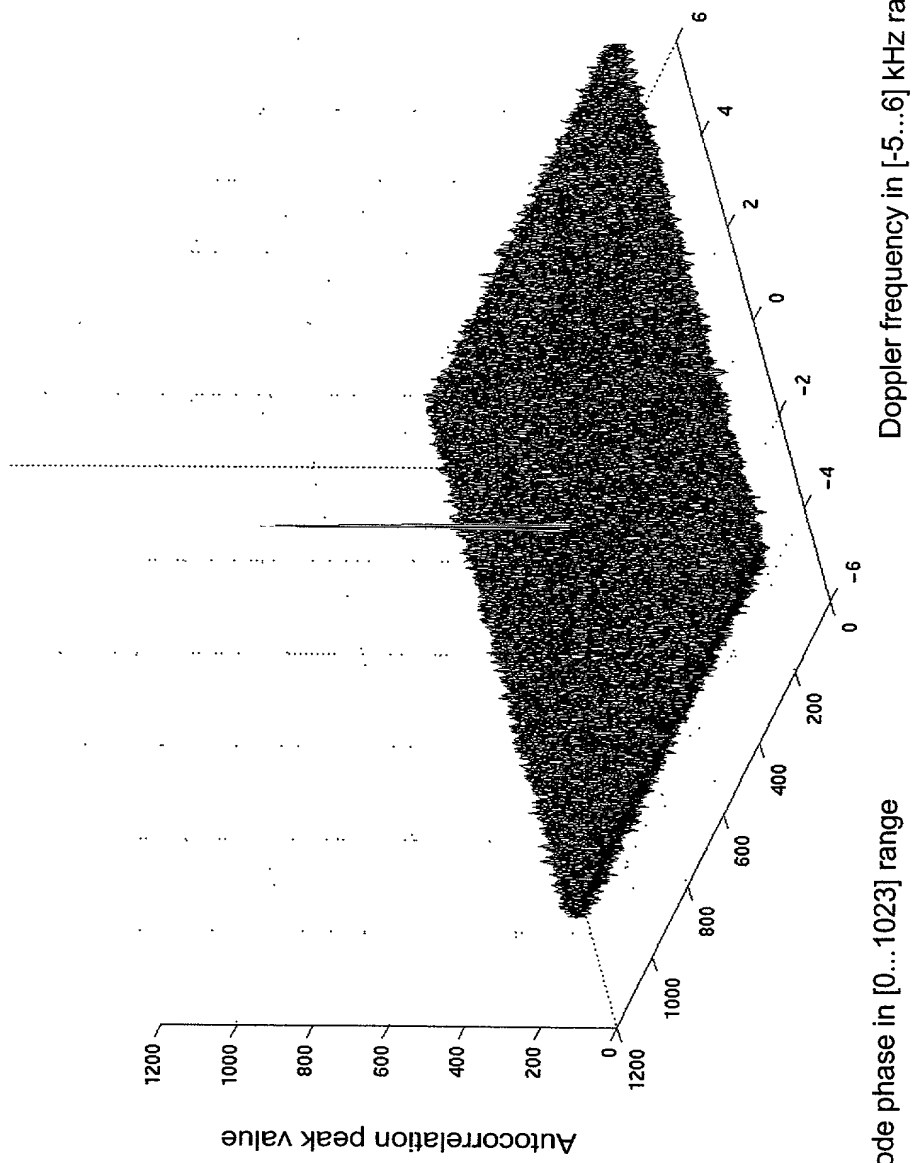


Fig. 10

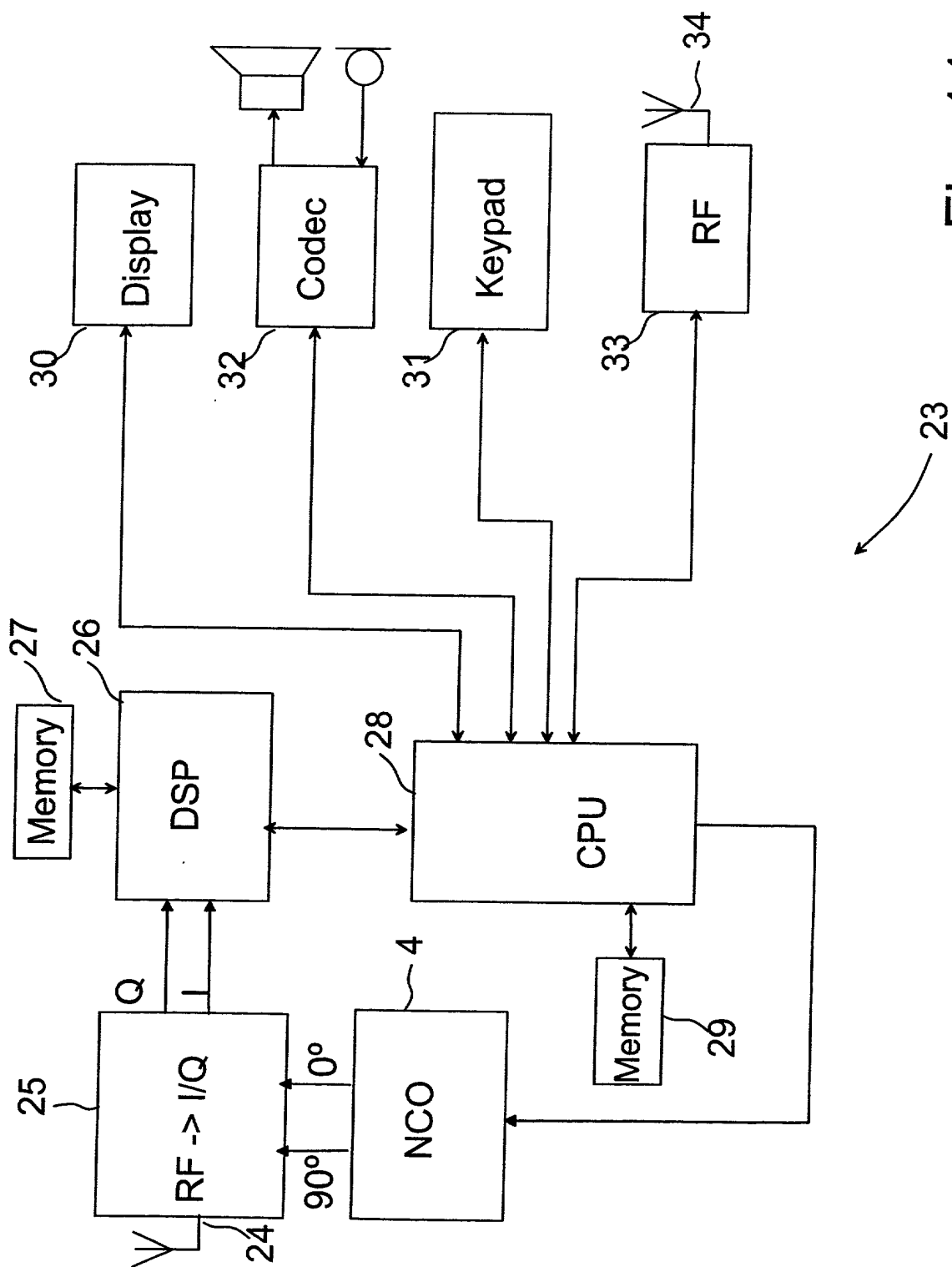


Fig. 11